COMPACT LOW-POWER 2.4 GHz QPSK MODULATOR IN CMOS

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ABSTRACT: *A compact low-power QPSK modulator is proposed for short-range wireless communications using a new pass-transistor logic circuit. It is experimentally demonstrated in the unlicensed 2.4 GHz ISM frequency band using standard 0.18 μm CMOS technology, with the data rates well exceeding 100 Mbps. The core circuit occupies only 505 μm by 435 μm and consumes less than 19 mW from 1.8 V.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1344–1348, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24300

Key words: *digital modulation; quadrature phase shift keying; CMOS; microwave integrated circuits; short-range wireless communications*

1. INTRODUCTION

Gigahertz-range quadrature phase shift-keying (QPSK) modulators have been studied extensively in the literature [1-6]. Most of the reported work generates quadrature signals using frequency divide-by-two circuits (DTCs) [1, 2], or resistor-capacitor, capacitor-resistor (RC-CR) networks with several cascaded stages of amplitude limiters [5–7]. This is usually followed by a pair of Gilbert-cell mixers and a summing junction to modulate and combine the quadrature carriers [1–4, 7, 8]. Such an approach can significantly augment the Integrated Circuit (IC) size, cost, and power consumption. In addition, some of the work was demonstrated in more expensive technologies such as Gallium Arsenide (GaAs), Silicon Bipolar, or BiCMOS.

In this article, a novel CMOS QPSK modulator is proposed using a Pass-Transistor Logic (PTL) network. A major advantage of this topology is its moderate circuit complexity and power consumption compared with other modulators. The concept proposed here builds on our previous work in Ref. 9, but we introduce a new structure and PTL circuit that offers significant improvements in size, power, modulation accuracy, and data rates [10]. The proposed circuit is experimentally demonstrated by directly modulating a 2.4 GHz signal. An accurate phase and amplitude balance is achieved after tuning the 90° phase shifter, with the errors being less than 1.4° and 0.3 dB, respectively. The measured data rates for this modulator reach the 200 Mbps range, whereas the carrier rejection achieved is more than 32 dB. The IC is implemented using a standard 0.18 μm CMOS process, measuring 720 μm by 888 μm and consuming 34 mW of power from a 1.8 V supply. This includes an active input balun and an output buffer integrated on-chip, without which the core circuit area is only 505 μm by 435 μm, and the estimated power consumption is less than 19 mW. The modulator is suitable for future short-range low-power wireless applications using either a direct-conversion architecture with a 2.4 GHz carrier or in a heterodyne architecture with a 38 GHz carrier as in point-to-point radio, for example, and a 2.4 GHz intermediate frequency (IF).

Whereas, QPSK modulation is predominantly used in heterodyne radio architectures, this modulation scheme is also convenient for use in direct-conversion radio systems because its moderate complexity enables the design of very high data rate demodulators at the carrier frequency. A well-known merit of direct-conversion transceivers is the absence IF oscillators, bandpass filters, and amplifiers, which substantially reduces the size and power consumption of the IC's in the physical layer. Furthermore, very high data rates are possible with the direct-conversion approach since the frequency bandwidth is no longer limited by a relatively low IF. However, direct-conversion transmitters can suffer from injection pulling, i.e., corruption of the carrier local oscillator (LO) frequency by the power amplifier (PA) output. Such a problem can be alleviated nonetheless by various shielding techniques to isolate the carrier LO [11–13] or by offsetting the LO frequency [14].

The article is organized as follows: Section 2 describes the principle operation and design of the circuit, Section 3 discusses the experimental results, and Section 4 concludes the work.

2. CIRCUIT ARCHITECTURE AND DESIGN

A block diagram of the QPSK modulator is shown in Figure 1. It consists of the following: (1) a 180° balun, (2) a 90° phase shifter, and (3) a switch network. The 180° balun and the 90° phase shifter

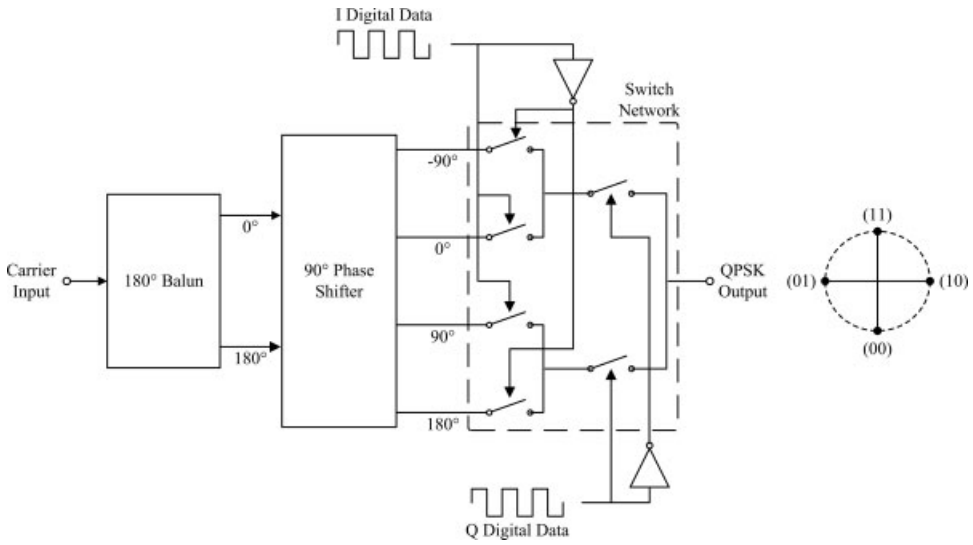

Figure 1 Block diagram of proposed QPSK modulator

generate all four quadrature phases of the carrier: 0°, −90°, 90°, and 180°. Only one of these is selected in the switch network according to both in-phase (I) and quadrature-phase (Q) digital data, which constitute the QPSK symbol value. In effect, the circuit performs QPSK modulation with the signal constellation shown in Figure 1. This architecture requires only one balun and no summing junction compared with our previous work [9], saving significant space and power. Furthermore, the parasitic coupling and nonidealities associated with the summing junction are no longer present, enabling higher modulation accuracy and data rate [10].

An active common-gate/common-source (CG-CS) pair balun [9, 10, 15] is integrated in the QPSK modulator IC to create differential signals from the off-chip single-ended oscillator. Active baluns are more easily integrated than passive baluns such as centre-tapped transformers [16–19], which can be prohibitively large in the S-band frequency range. The CG-CS active balun also exhibits a low input reflection coefficient and a good phase and amplitude match over a wide band of frequencies [9, 10, 15]. The outputs of the balun are also buffered using source followers to sufficiently drive the following 90° phase shifter with relatively low impedance [10]. Note that the QPSK modulator can also be used directly with the on-chip differential oscillator commonly found in integrated transmitters without the need for a balun.

2.1. Quadrature Phase Shifter

The QPSK modulator signal constellation accuracy and modulation bandwidth depends highly on the accuracy of creating quadrature phases. For this reason, several techniques have been developed over time to generate accurate 90° phase shifters with low phase and amplitude errors. These include the following: (1) frequency divide-by-two circuits (DTCs) [1, 2, 20]; (2) resistor-capacitor, capacitor-resistor (RC-CR) networks [4-6]; (3) resistor-capacitor (RC) all-pass filters [3, 21]; (4) inductor-capacitor (LC) high- and low-pass filters [22–24]; and (5) RC polyphase networks [25–29].

A single-stage tunable RC polyphase network is used in this design due to its small IC footprint and zero DC power consumption compared with the other networks. It also has less signal loss than using two RC-CR circuits, as it combines the two balanced signals as opposed to splitting each signal separately. Figure 2 shows the polyphase network and how it operates [10]. It generally has an all-pass frequency response (unity gain) while shifting the differential inputs by ±45° toward each other at the $1/(RC)$ cut-off frequency and forming the required differential quadrature phases upon combination at the outputs. Therefore, for the relatively high S-band frequency range, a small RC product is required allowing small resistors and capacitors to be used. However, integrated

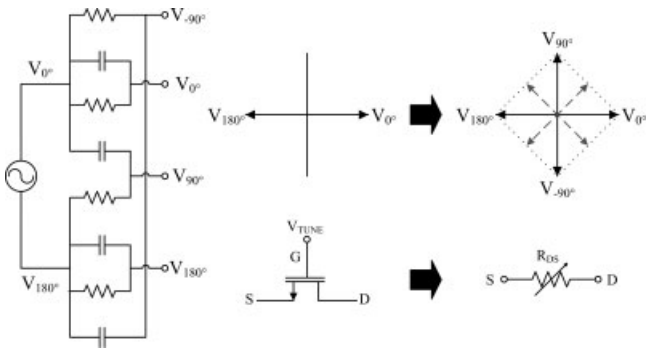

Figure 2 RC polyphase network and NMOS FET resistor operation

polysilicon resistors can generally exhibit large tolerances (on the order of 20% or more) for small footprints and low resistance values (less than 1 kΩ). Such high tolerances are critical since discrepancies will change the cutoff frequency, introducing phase errors at the frequency of interest. For this reason, a variable resistor in the form of a zero-biased NMOS transistor is used, with the resistance controlled by the gate voltage V_{TUNE} (Fig. 2). This way the cutoff frequency can now be tuned to the carrier frequency after process variations for the lowest possible phase error.

The effective resistance R_{DS} of the zero-biased NMOS device is well-known to be approximately given by the following:

$$R_{\mathrm{DS}} = \left(\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{DS}}}\right)^{-1} \approx \frac{1}{\mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{T}})} = \frac{1}{\mu_n C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{TUNE}} V_{\mathrm{T}})} \quad (1)$$

where, μ_{n} is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the transistor, V_{GS} is the gate-source voltage and V_{T} is the threshold voltage. It is clear that the resistance is inversely proportional to the tuning voltage and gate width, thus a large voltage or width can be used to yield a relatively low resistance. However, a larger device width will increase the parasitic capacitances, leading to a higher signal loss and degrading the performance. For this reason, the gate width is made narrow while the tuning voltage is increased in proportion for the same resistance. The larger gate overdrive voltage also helps to extend the linearity of the transistor and reduce signal distortion [10].

The cutoff frequency of the polyphase network ($1/(RC)$) was chosen to be 2.4 GHz for this QPSK modulator. This is an unlicensed ISM frequency band widely used for wireless communication devices. The capacitance C in the polyphase network was set to a relatively small value of 0.1 pF to minimize its IC footprint. With $C = 0.1$ pF, the required resistance is $R = 660\ \Omega$. An NMOS FET with a narrow gate width of $W = 1.5\ \mu$m is used to implement this resistance with a low parasitic capacitance. For the 0.18 μm CMOS technology used, the device parameters are as follows: $\mu_{\mathrm{n}} = 4.38 \times 10^{-2}$ m^2/Vs, $C_{\mathrm{ox}} = 8.03 \times 10^{-3}$ F/m, $V_{\mathrm{T}} = 0.475$ V and $L = 0.18\ \mu$m. Therefore, from (1), the required tuning voltage is $V_{\mathrm{TUNE}} = 0.99$ V. An S-parameter simulation was also run to verify this, indicating a resistance value of about 650 Ω.

The differential quadrature outputs V_{-90}, V_0, V_{90}, and V_{180} of the RC polyphase network (Fig. 2) are amplified using common-source amplifiers. This isolates the RC polyphase network from the following switch network, presenting consistent loading impedance to the four outputs regardless of the switching state to ensure good quadrature phase and amplitude match.

An S-parameter simulation was run to verify the performance of the RC polyphase network, and the phase of the resulting transmission coefficients is plotted in Figure 3. As shown, the phase differences between the outputs are very close to the desired 90°, 180°, and 270° (−90°) at 2.4 GHz, with a phase error of less than 0.08°. The magnitudes of these transmission coefficients also indicate a low amplitude imbalance of 0.071 dB at the same frequency.

2.2. Switch Network

The purpose of the switch network is to pass one signal from the four differential quadrature signals (V_{-90}, V_0, V_{90}, and V_{180}), whereas blocking the other three, according to both I and Q data values which constitute the QPSK symbol. In particular, the following digital logic should be realized by the switch network to

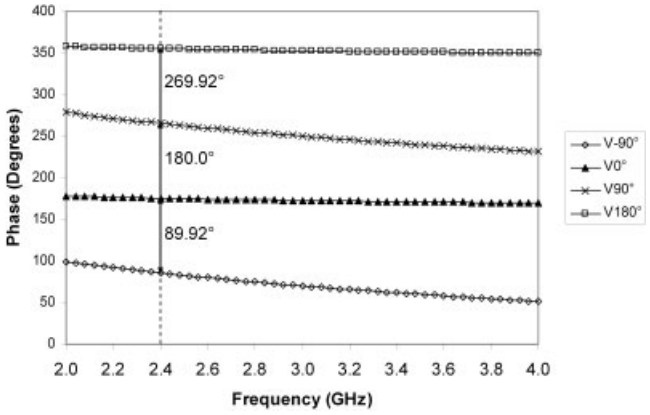

Figure 3 Simulated transmission coefficient phase for RC polyphase network at 2.4 GHz

yield the desired QPSK signal constellation at the output (V_{QPSK}) as follows:

$$V_{QPSK} = IQV_{-90} + IQV_0 + IQV_{90} + IQV_{180} = Q(IV_{-90} + IV_0) + Q(IV_{90} + IV_{180}) \quad (2)$$

This is realized in Figure 1 as a set of six complimentary switches in two stages, the first four being for the I data stream and the remaining two for the Q data stream. A Pass-Transistor Logic (PTL) circuit consisting of six NMOS switches, as shown in Figure 4, is used to implement this, which has the advantages of small footprint, zero DC power consumption, and high-speed operation. In the ON state, the device can be characterized with the on-resistance given by (1), where the applied gate-source voltage V_{GS} is equal to the supply voltage V_{DD}.

While increasing the FET width W will reduce its on-resistance and thus the signal loss across it, it will also increase its parasitic capacitances. This leads to more capacitive coupling between the data and carrier signals as well as less isolation in the OFF state, adversely affecting the performance of the QPSK modulator. Therefore, a narrow gate width of $W = 1.5$ μm was chosen for this design to minimize this effect, especially at higher data rates where it is more pronounced. To maintain circuit symmetry with respect to the I and Q data inputs, transistors M5 and M6 are made twice as wide as transistors M1–M4 with $W = 3$ μm.

The QPSK signal output V_{QPSK} of the PTL circuit (Fig. 4) is buffered using a source follower to sufficiently drive the external 50 Ω load with a low insertion loss and reflection coefficient. The buffer offers a wideband impedance match in comparison to using

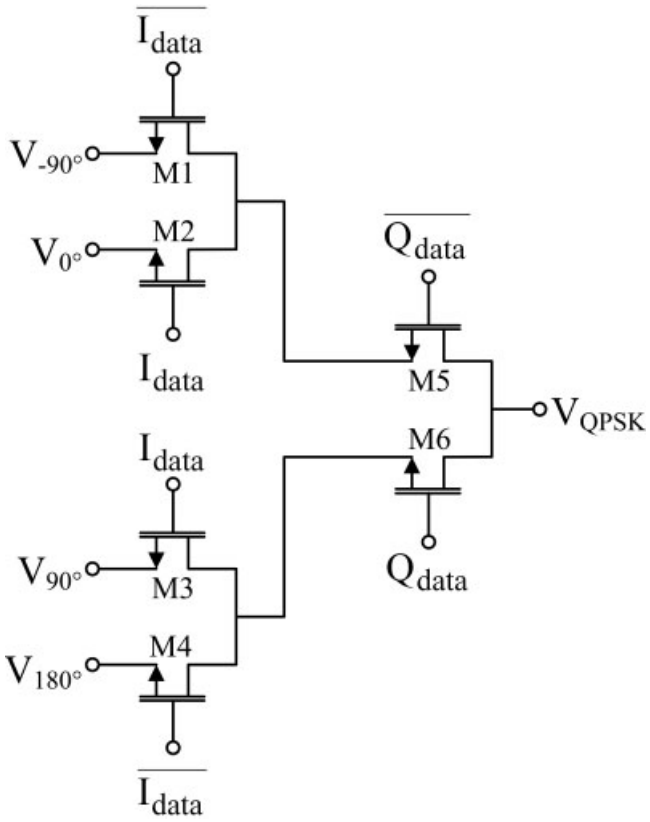

Figure 4 Circuit schematic of PTL circuit for QPSK modulator

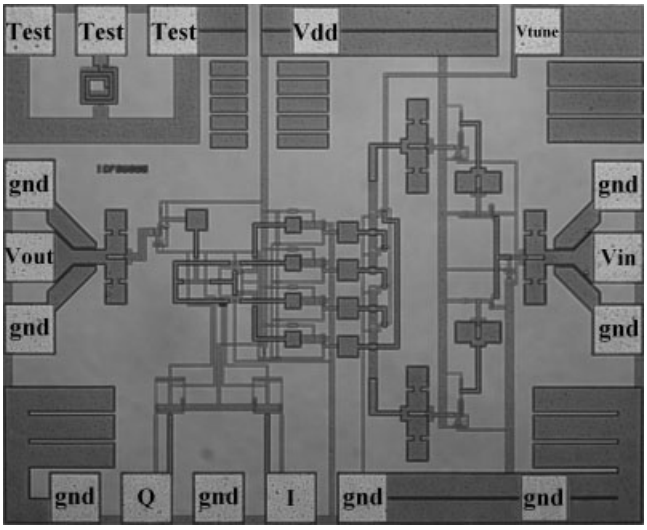

Figure 5 Photograph of the QPSK modulator IC

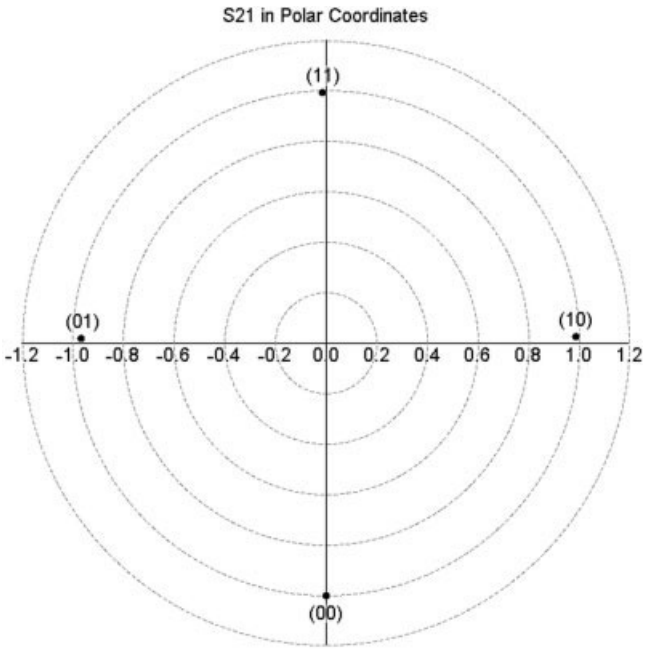

Figure 6 Measured static constellation of the QPSK modulator

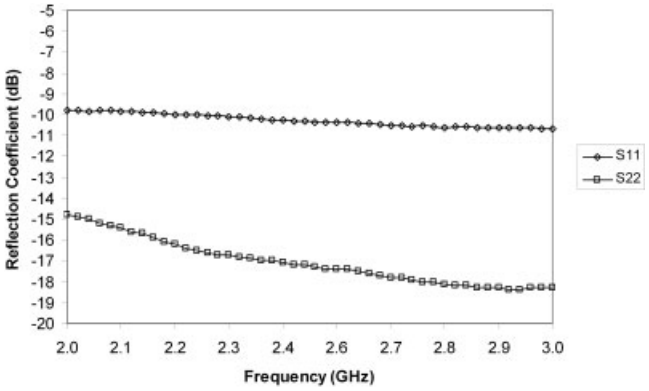

Figure 7 Measured input S_{11} and output S_{22} reflection coefficient

a narrowband passive network which would also be prohibitively large in this frequency range.

3. EXPERIMENTAL RESULTS

The QPSK modulator was fabricated in a standard (six-metal, single-poly) 0.18 μm CMOS process. A photograph of the IC is shown in Figure 5. It occupies a die area of about 0.720 $\times$ 0.888 mm^2, including bonding pads, and consumes 34 mW of power from a 1.8 V supply. Without the input balun and the output buffer, the core circuit area is only 0.505 $\times$ 0.435 mm^2 and the estimated power consumption is less than 19 mW.

The first measurement performed was the static constellation of the modulator with the I and Q data switches held at constant values corresponding to the four QPSK symbols (00, 10, 11, and 10). A polar plot of the normalized transmission coefficient S_{21} at 2.4 GHz in each of the four states is shown in Figure 6. The maximum phase and amplitude errors are only 1.4° and 0.3 dB, respectively. In addition, the magnitude of this transmission coefficient indicates a maximum loss of less than 5.5 dB. These measurements were performed with the tuning voltage V_{TUNE} set to about 0.7 V, as this was found to give the smallest errors at 2.4 GHz. The measurements also reasonably agree with the simulations.

The input S_{11} and output S_{22} reflection coefficients were also measured and a plot of their magnitude is shown in Figure 7. At the centre frequency of 2.4 GHz, the input and output reflection coefficients are less than -10 and -17 dB, respectively. These results are sufficiently low as desired, agreeing closely with our simulations.

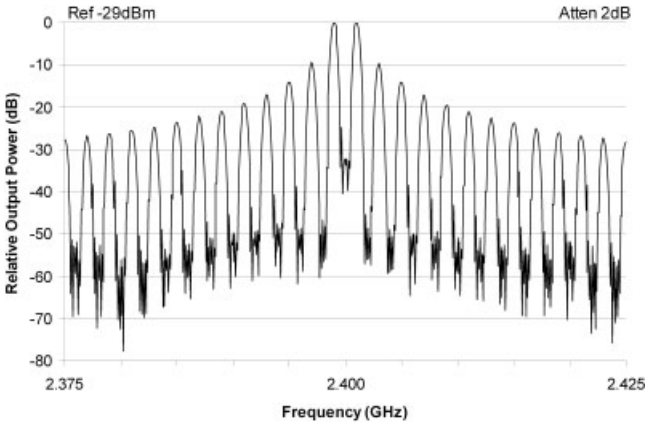

Figure 8 Measured carrier rejection with 1 MHz square wave

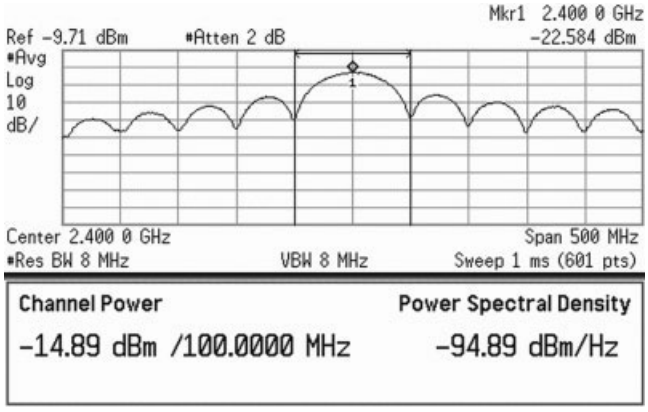

Figure 9 Measured output QPSK spectrum for 100 Mbps

To measure the QPSK modulator's carrier rejection, the same square wave is applied to both I and Q data channels and the output frequency spectrum is examined. The frequency of the square wave f_{MOD} was chosen to be 1 MHz. This corresponds to a 2 Mbps data rate per channel or a total throughput of 4 Mbps. The spectrum of an ideal periodic square wave has nonzero components only at the odd-order harmonics of the fundamental frequency (1, 3, 5 MHz, etc.), featuring a sinc-shaped amplitude envelope. Figure 8 shows the output signal spectrum with a frequency span of 50 MHz. The depicted spectrum shape is as expected and the 2.4 GHz carrier is well suppressed by more than 30 dB relative to the main lobes at 2.4 GHz $\pm$1 MHz. The carrier input power for this test was set to -20 dBm. For a higher input power of -10 dBm, the carrier rejection remains largely unchanged at about 28 dB.

Tests were also performed using pseudo-random binary sequences (PRBS) for the input I and Q channels. The sequences were encoded in the non-return-to-zero (NRZ) format with rectangular pulses. Their data rate f_{MOD} was maximized to 50 and 100 Mbps for a total data throughput of 100 and 200 Mbps, respectively. Figures 9 and 10 show the resulting output signal spectra with a centre frequency of 2.4 GHz and frequency spans of 500 MHz and 1 GHz, respectively. It is evident that the circuit operates as a QPSK modulator with its generated spectra closely matching the theoretical one without pulse shaping. Finally, the measured output power is about -15 dBm for -10 dBm input power as indicated on the plots.

Table 1 summarizes the measured characteristics of the QPSK modulator IC.

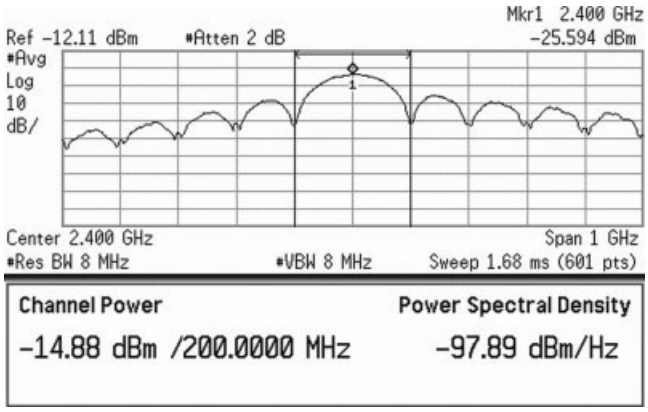

Figure 10 Measured output QPSK spectrum for 200 Mbps

TABLE 1 Summary of Measured Characteristics of QPSK Modulator IC

Characteristic	Results
Circuit area	0.505×0.435 mm^2
DC power	19 mW from 1.8 V
Carrier frequency	2.4 GHz
Accuracy	Amplitude error $\leq$ 0.3 dB Phase error $\leq 1.4°$
Insertion loss	$\leq$5.5 dB
Return loss	Input: $\geq$10 dB Output: $\geq$17 dB
Carrier rejection	$\geq$30 dB
Data throughput	Nominal: 100 Mbps Maximum: 200 Mbps
Output power	-15 dBm

4. CONCLUSIONS

A compact low-power QPSK modulator has been proposed in CMOS for short-range wireless applications. An RC polyphase network is employed to generate balanced quadrature signals for its small footprint and zero DC power consumption, with variable NMOS resistors tuned after fabrication to minimize phase errors. Only one of the four differential quadrature signals is selected by a new PTL circuit according to both *I* and *Q* digital data, thus eliminating the need for a summing junction. The circuit is demonstrated at 2.4 GHz in a standard 0.18 μm CMOS process, with the data rates reaching 200 Mbps and the carrier rejection exceeding 30 dB. An accurate phase and amplitude balance is achieved with the errors being less than 1.4° and 0.3 dB, respectively. The insertion loss is also lower than 5.5 dB, whereas the input and output return losses are better than 10 dB. The core circuit occupies an area of only 0.505×0.435 mm^2 and consumes less than 19 mW of power.

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HYBRID IPO-BI-FEM FOR THE ANALYSIS OF 2D LARGE RADOME WITH COMPLEX STRUCTURE

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ABSTRACT: *In this article, the iterative physical optics-boundary integral-finite element method (IPO-BI-FEM) is proposed for the analysis of*